The invention claimed is:

1. A circuit device having an external resistor for establishing a delay of a signal relative to another signal of the circuit.

2. A semiconductor device comprising:

an integrated circuit buffer that receives an input signal and generates a plurality of output signals that relate to the input signal, wherein the buffer includes a delay generator; and

a resistor having a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference, wherein the resistor is external to the integrated circuit buffer.

3. The device of claim 2 wherein the buffer comprises a zero-delay buffer.

4. The device of claim 2 wherein the device is implemented on a circuit board and the external resistor is connected to a pin on a device package.

5. The device of claim 2 further comprising a plurality of internal capacitors which are used in conjunction with an external resistor for providing a timing reference, each capacitor having a first capacitor end that is electrically connected to a current source and a second capacitor end that is electrically connected to ground or a voltage reference.

6. The device of claim 2 wherein:

the buffer further includes a phase locked loop, the phase locked loop includes a phase detector; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of an internal feedback signal before the feedback signal reaches the phase detector.

7. The device of claim 6 wherein the plurality of output signals are phase-shifted to have a timing that is advanced relative to the input signal.

8. The device of claim 7 wherein a magnitude of the phase-shift is dependent upon the value of the external resistor.

9. The device of claim 2, wherein:

the buffer further includes a phase locked loop, the phase locked loop includes a phase detector; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of the input signal before the input signal reaches the phase detector.

10. The device of claim 9 wherein the plurality of output signals are phase-shifted to have a timing that is retarded relative to the input signal.

11. The device of claim 10 wherein a magnitude of the phase-shift is dependent upon a value of the external resistor.

12. The device of claim 2 wherein:

the buffer includes a phase locked loop; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of one or more of the output signals exiting the phase locked loop to yield adjusted output signals.

13. The device of claim 12 wherein the adjusted output signals are phase-shifted to have a timing that is advanced or retarded relative to the input signal and the remaining output signals.

14. The device of claim 13 wherein a magnitude of the phase-shift is dependent upon a value of the external resistor.

15. A method of adjusting the timing of an output signal of a semiconductor device, comprising:

electrically connecting a first terminal of an external resistor to a buffer that generates a plurality of output signals; and

electrically connecting a second terminal of the external resistor to a ground or a voltage reference;

wherein the buffer includes a delay generator and a phase locked loop, and the first terminal of the external resistor is electrically connected to the delay generator to adjust the

timing of one or more of the output signals in an amount that is dependent upon the value of the external resistor.

16. The method of claim 15 wherein the buffer comprises a zero-delay buffer.

17. A semiconductor device, comprising

an input terminal for receiving an input signal;

a buffer for generating a plurality of output signals; and

an external resistor for altering a timing of one or more of the plurality of output signals relative to a timing of the input signal.

18. The device of claim 17 wherein the buffer comprises a zero-delay buffer.

19. The device of claim 18 wherein the device is implemented on a circuit board and the external resistor is connected to a pin on a package of the device.

20. The device of claim 18 wherein the adjusted output signals are phase-shifted to have a timing that is advanced or retarded relative to the input signal and the remaining output signals.

21. The device of claim 18 wherein a magnitude of the phase-shift is dependent upon a value of the external resistor.